UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/619,704	07/15/2003	Ji Yon Kim	CU-3272 RJS	7160

26530 7590 06/15/2005

LADAS & PARRY LLP
224 SOUTH MICHIGAN AVENUE
SUITE 1600
CHICAGO, IL 60604

EXAMINER	
DINH, TUAN T	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 06/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/619,704	KIM, JI YON	
	Examiner	Art Unit	
	Tuan T. Dinh	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,16,29 and 30* is/are rejected.

7)☒ Claim(s) *3-15 and 17-28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08/15/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a) because they fail to show: "a circuit pattern, a lead frame, an external device, a conductive bump, conductive frame is coated with a conductive material, a tape automated bonding (TBA) tape, PCB comprises... ball lands, and solder balls" as claimed from claims through claim 30 as described in the specification. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Examiner suggest applicant providing more details of any claimed elements in the drawings for better exam.

Specification

2. The disclosure is objected to because of the following informalities:

Page 13, line 9, page 14, line 5, page 16, line 8, please correct the mistypes of the range.

Appropriate correction is required.

Claim Objections

3. Claims 8, 22 are objected to because of the following informalities:

Claims 8 and 22, line 3, it is unclear. What does applicant mean of "an alloy 42"? Is it a trademark name? Please correct.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-2,16, and 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Happoya (U.S. Patent 6,084,780) in view of Papageorge et al (U.S. Patent 5,438,224).

As to claim 1, Happoya discloses a stack-type semiconductor package (10, column 4, line 13) having one or more semiconductor devices (18, 32) contained therein as shown in figures 6-9 comprising:

a printed circuit board (PCB-12, column 4, lines 15-16) having a circuit pattern (16, column 4, line 16);

a first device (18, column 4, lines 16-17) stacked on the PCB (12) and electrically connected to the PCB circuit pattern (terminals of the device 18 connected to pads 14 of the PCB 12, see column 4, lines 22-26);

a conductive frame (24, column 4, lines 28-30) having first and second terminals (27, 26, column 4, lines 34-35), wherein the first terminals (27) are electrically connected to the PCB circuit pattern (16), see column 4, lines 48-55); and

a second device (32, column 4, line 40) stacked on the conductive frame (24) over the first device (18) and electrically connected to second terminals (26) of the conductive frame (24),

wherein the second device (32) is electrically connected to the PCB circuit pattern (16) and the first device (18) via the conductive frame (24).

Happoya does not specifically disclose the first and second devices, which are first and second semiconductor memory devices.

Papageorge et al. teaches a stacked of integrated chip arrangement as shown in figures 1-3 comprising first and second memory IC's (110, 120, column 2, lines 58-68).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have memory IC's as taught by Papageorge et al, modified the

devices of Happoya for the purpose of increasing memory capacitances for the package.

As to claim 29, Happoya discloses a stack-type semiconductor package as shown in figures 6-9 comprising:

a printed circuit board (PCB 12) having a circuit pattern (16), wherein one or more semiconductor devices (18, 32) are stackable on the PCB;

a first package (18) stacked on the PCB and electrically connected to the PCB circuit pattern (16);

a second package (32) stacked above the first package (18); and

means for (24) providing electrical connection (26, 27) between the second package (32) and the PCB circuit pattern (16) and between the second package (32) and the first package (18).

Happoya does not specifically disclose the first and second packages, which are first and second semiconductor memory packages.

Papageorge et al. teaches a stacked of integrated chip arrangement as shown in figures 1-3 comprising first and second memory IC's (110, 120, column 2, lines 58-68).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have memory IC's as taught by Papageorge et al, modified the devices of Happoya for the purpose of increasing memory capacitances for the package.

As to claims 2 and 30, Happoya does not disclose each of the first and second devices is a ball grid array type stack package (BGA package) having a plurality of solder balls at its lower surface.

Papageorge et al. shows the two IC's (110, 120) are BGA packages having solder balls at lower surfaces, see column 3, lines 22-31.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have BGA packages as taught by Papageorge et al. modified the devices of Happoya in order to reduce mounting area and improve electrical characteristics.

As to claim 16, Happoya discloses the first device (18) is a thin-small-outline-package-type semiconductor package (TSOP package) having a plurality of TSOP leads (20) for electrical connection to the PCB circuit pattern (16). Happoya does not disclose the second device is a ball grid array type stack package (BGA package) having a plurality of solder balls at its lower surface.

Papageorge et al. shows an memory IC chip (120) of a arrangement (140) as shown in figure 1, which is a BGA chip.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have BGA packages as taught by Papageorge et al. modified the devices of Happoya in order to reduce mounting area and improve electrical characteristics.

Allowable Subject Matter

6. Claims 3-15, and 17-28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Neither the references cited nor the cited references does disclose the limitations of claims 3, 10, 17, and 24.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. McIver, Wang et al., and Kledzik et al. disclose related art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Dinh whose telephone number is 571-272-1929. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan Dinh
June 07, 2005.